On page 1, line 2, please **insert** the following paragraph:

This application is a continuation of Application No. 09/561,868, filed on May 1, 2000 (pending); which is a continuation of Application No. 09/480,767, filed on January 10, 2000(pending); which is a continuation of Application No. 08/979,402 (now U.S. Patent 6,122,688), filed on November 26, 1997; which is a division of application No. 08/545,292 filed on October 19, 1995 (now U.S. Patent 5,748,914).

A1

Please **substitute** the paragraph starting on page 16, line 19, with the following paragraph:

A2

At step 814, the data is transmitted over the data bus (BusData[8:0]). During this step, the data may be transmitted to or from the target DRAM, depending on whether the data transfer operation is write or read operation. At some fixed period of time prior to the transmission of the last data packet, the controller transmits the terminate signal on the BusCtl line (step 816). Steps 816 and 814 are shown as a single step 812 to indicate that step 816 is performed during the performance of step 814.

Please **substitute** the paragraph starting on page 17, line 4, with the following paragraph:

A3

As shall be explained below, one embodiment of the memory controller dynamically adjusts the interleave of data and control information to more fully utilize the channel. Interleave refers to the relative ordering of data, requests and control signals that are associated to multiple transactions. To allow dynamic

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